REMARKS

1. The Examiner has rejected claims 1-6 and 8-12 under 35 U.S.C. § 103(a) as being unpatentable over Burns et al. (U.S. Patent No. 6,683,498) in view of Vice (U.S. Patent Application Publication No. 2005/0062533). Further, the Examiner has rejected claims 7 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Burns et al. in view of Vice, and further in view of Brown (U.S. Patent No. 6,194,972). These rejections are respectfully traversed, and further consideration is requested. The amendments presented herein are believed to place the claims in better form for consideration on appeal, and were not sooner presented because the Applicant did not fully appreciate the manner in which the cited references were applied to the previously presented claims. Thus, the Applicant respectfully requests the amendments presented herein be entered.

2. The Examiner has rejected claims 1-6 and 8-12 under 35 U.S.C. § 103(a) as being unpatentable over Burns et al. in view of Vice. Applicant's amended claim 1 is an independent claim directed toward a differential transistor pair having resistive load elements coupled to their collectors, with mutually coupled inductors coupled in series with each of the resistive load elements to form a transformer having windings connected out of phase with the resistive load elements in such a way that that an inverted falling edge waveform at a node associated with the first resistive load element is coupled to a rising edge waveform at a node associated with the second resistive load element, substantially equalizing waveform rise and fall times.

The Burns et al. reference is directed toward a protection circuit designed to extend headroom with off-chip inductors. There is never any illustration or discussion of mutual

inductance, although series-connected inductor/resistor circuits are shown as loads in some illustrations of the amplifier circuit. It seems clear, particularly after a look at the parent application, that the series RL circuits are intended as loads. The parent case notes that the "spirals" (inductors) are used for gain enhancement and may be omitted if a faster IC process is used. This is a clear reference to the known expedient of placing inductors in series with the load resistors of the differential pair output stages, where self-inductance of the inductors is chosen to add to the load impedance near the 3dB point of the amplifier's frequency response, thus extending the bandwidth. This works because the series RL circuit maintains the load impedance beyond the normal 3dB frequency.

The Vice reference is directed toward a coupled-inductance differential amplifier. The coupled inductors are used for biasing the transistors and for providing impedance matching at the output ports (See paragraph [0011] of Vice). This type of impedance match is well-known in applications where the circuit operates at a single frequency of interest and it is desired to match output impedance to load for maximum power transfer. The circuits illustrated and described in Vice do not include any series resistance in the drain circuits of the differential pair.

Furthermore, according to the applicant's specification, in high-speed applications, collector time constant can be a significant limitation on bandwidth. Collector capacitance acts as a shunt in parallel with the load resistor. One can move the pole associated with the collector node by reducing collector load resistance and increasing operating current. However, this results in increased power dissipation, and temperature rise causes transistor parameters to deteriorate. Consequently, mere reduction of load resistance is not a preferred solution. Instead, the present invention contemplates adding a series inductance in series with each collector load

resistance for each transistor in the differential pair, and coupling the series inductors together by mutual inductance.

In the present invention, the two inductors coupled together form a transformer whose windings are connected out of phase with the load resistors. Thus, the configuration forms a highly damped dual parallel resonant circuit. The use of mutual inductance allows the inductance of each individual winding to be reduced, resulting in a more compact layout. And, since the inverted falling edge waveform is coupled to the other rising edge node, rise and fall times are equalized in the coupled inductor configuration of the present invention. This is very beneficial in switching applications.

Neither Burns et al. nor Vice teaches or suggests the inventive combination recited in applicant's claim 1, nor does Burns et al. or Vice discuss these design considerations. Consequently, there is no teaching or suggestion that supports combination of these two references. Burns et al. and Vice were simply combined based upon hindsight, with full knowledge of applicant's claimed invention. Thus, for the reasons set forth above, the applicant respectfully submits that claim 1 is patentably distinguishable over the prior art of record, and should thus be passed to allowance.

Claim 2 depends from claim 1, which has been shown to be allowable above, and is consequently allowable because it depends from an allowable base claim. In addition, the essential limitations of claim 2 introduce patentable subject matter, particularly when considered in light of the base claim, and should thus be passed to issuance for this additional reason.

Claim 3 is an independent claim that recites essentially the same limitations found in claim 1, except that claim 3 is not recited as an improvement-style claim. For the same reasons set forth above with respect to claim 1, the applicant respectfully submits that claim 3 is also in

condition for allowance, and should thus be passed to issuance. Claims 4 through 7 depend ultimately from claim 3, which has been demonstrated to be allowable, and should thus be passed to issuance as depending from an allowable base claim.

Claim 8 is an independent method claim reciting a method for extending the bandwidth of a differential pair that has resistive load elements coupled to its collectors. The method steps include connecting an inductor in series with each of the resistive load elements and magnetically coupling the inductors together. Since the method steps of claim 8 are closely analogous to the structural limitations recited in claim 1, the applicant respectfully submits that claim 8 is in condition for allowance for the same reasons set forth above in conjunction with claim 1.

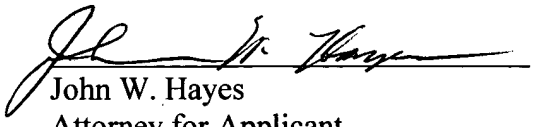
Claim 9 is an independent claim that recites similar subject matter to that recited in claim 1, except that the mutually coupled inductors in series with the load resistors are recited as a transformer. Thus, the applicant respectfully submits that claim 9 is in condition for allowance for the same reasons set forth above in the discussion of claim 1. Claims 10 through 12 depend ultimately from claim 9, which has been shown to be allowable, and are thus also in condition for allowance.

3. The Examiner has rejected claims 7 and 13 under 35 U.S.C. § 103(a) as being unpatentable over Burns et al. in view of Vice, and further in view of Brown (U.S. Patent No. 6,194,972). The Brown reference is directed toward a gyrator design in which loop amplifiers are connected to inductive elements. Contrary to the Examiner's assertion regarding reduction of collector loading in Brown, it seems more likely that the buffers in Brown are intended to limit the impact of the load on the oscillator frequency of the gyrator circuit. In addition, claim 7

depends ultimately from claim 3, which has been shown to be allowable, and thus claim 7 should also be passed to issuance as depending from an allowable base claim. The same is true of claim 13, which depends from claim 9, shown allowable above.

4. In view of the above amendments and remarks, allowance of all claims pending is respectfully requested. If a telephone conference would be of assistance in advancing the prosecution of this application, the Examiner is invited to call applicant's attorney.

Respectfully submitted,



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